CLAIMS

1. A system for digital system performance enhancement that receives an input signal and a first clock signal, said system comprising:

clock control logic that receives the first clock signal and generates a second clock signal and a third clock signal, wherein said second and third clock signals have a frequency that this an integer fraction of the first clock signal frequency;

a first digital synchronous network responsive to the first clock signal and the input signal, and provides a first output signal;

a second digital synchronous network substantially identical to said first digital synchronous network, wherein said second digital synchronous network receives said second clock signal and the input signal, and provides a second output signal;

a third digital synchronous network substantially identical to said first digital synchronous network, wherein said third digital synchronous network receives said third clock signal and the input signal, and provides a third output signal; and

comparison and selection logic responsive to said first, second and third output signals to determine if a fault has occurred in the computation of said first output signal, wherein if a fault has not occurred said comparison and selection logic provides a system output signal indicative of said first output signal, wherein if a fault has occurred said comparison and selection logic provides said system output signal indicative of said second output signal.